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MOTOROLA
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PRODUCT INFORMATION

MC68341
MC68341V

Product Brief

Integrated CD-I Engine

The MC68341 is a member of the M68300 family of integrated processors designed specifically for the compact disc-interactive (CD-I) market. It improves on the feature set of the MC68340 for a more complete and cost effective integrated system solution to CD-I's specific needs.

The MC68341 contains a 68020-based CPU32, a two channel DMA controller, two serial channels, a timer, and a queued serial peripheral interface. The 68341's system integration module (SIM41) contains clock circuitry, system protection, external bus interface, timers, and additional chip selects. New to the SIM is the real time clock and an MC68000 bus interface. The MC68000 bus interface is dynamically selectable to give a glueless interface to peripherals and memory designed for the MC68000 while allowing higher performance transfers using the standard 68300 bus interface. Complete code compatibility with the MC68000 affords the designer access to a broad base of established real-time kernels, operating systems, languages, applications, and development tools—many oriented towards embedded control.

As a low voltage part, the MC68341V can operate with a 3.3-V power supply and is particularly useful for applications. MC68341 is used throughout this document to refer to both the low voltage and standard 5-V parts since both are functionally equivalent. Figure 1 illustrates a block diagram of the MC68341.

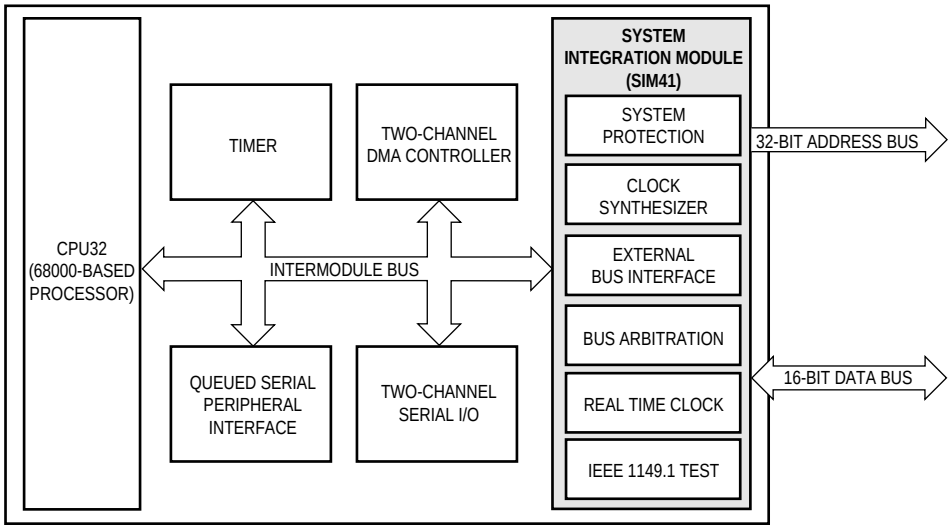

Figure 1. MC68341 Simplified Block Diagram

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MC68341 FEATURES

The primary features of the MC68341 are as follows:

- High Performance CPU32 Core Processor
  - — Upward Object-Code Compatible with MC68000 and MC68010
  - — Additional 32-Bit MC68020 Instructions and Addressing Modes
  - — Fast Two-Clock Register Instructions
- High-Speed Dual DMA Controllers for Low-Latency Transfers
  - — 50-Mbyte/Sec Sustained Transfer Rate
  - — Dual or Single Address Transfers
  - — 8-, 16-, or 32-Bit Transfers
- Counter/Timer
  - — 16-Bit Timer with 8-Bit Prescaler
  - — Multi-mode Operation
  - — 80 nS Resolution
- Dual Serial Communication Ports
  - — Synchronous or Asynchronous Operation
  - — 3-Mbit/Sec Sustained Transfer Rate
  - — Modem Control
  - — Baud Rate Generation
  - — 68681/261 Compatible
- Queued Serial Peripheral Interface (QSPI)
  - — Communications with Slow Peripherals without Tying Up the CPU
  - — Queued Transmit and Receive Buffers
  - — Programmable for Master or Slave SPI Operation
- System Integration Module for Flexible and Cost-Effective System Interface
  - — 32-Bit Address Bus; 16-Bit Data Bus with Dynamic Bus Sizing
  - — System Protection, Reset, and Configuration Control
  - — Periodic Interrupt/System Timer
  - — Chip-Select, Wait State Generation, Bus Watchdog
  - — Interrupt Controller
  - — IEEE 1149.1 Boundary Scan (JTAG)
  - — Dual 8-Bit Parallel Ports
  - — Real Time Clock
    - Time and Date with Leap Year Correction
    - Programmable Alarm for Interrupt or External Output
    - Calibration Register Eliminates Need for Trim Capacitor
    - Battery Backup Capability
- Power Management
  - — 5 V or 3.3 V Operation
  - — Fully Static HCMOS Technology
  - — Programmable Clock Synthesizer for Full Frequency Control
  - — Power-Down/Low Power Stop Capabilities
  - — Idle Modules Can Be Individually Powered Down
- 0–16 or 25 MHz Operation
- 160-Pin Plastic Quad Flat Pack (QFP)

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CENTRAL PROCESSING UNIT

The CPU32 is a powerful central processor that supervises system function, makes decisions, manipulates data, and directs I/O. A special debugging mode simplifies processor emulation during system debug.

CPU32

The CPU32 is a 68000-based microprocessor that can execute most 32-bit operations in two clock periods. Additional instructions enhance lookup table interpolation and power consumption control. In addition to performing basic instruction execution, the CPU32 provides a sophisticated background debug port for non-invasive instrumentation in the software development and debug environments.

ON-CHIP PERIPHERALS

To improve total system throughput and reduce part count, board size, and cost of system implementation, the M68300 family integrates on-chip, intelligent peripheral modules, and typical glue logic. These functions on the MC68341 include the SIM41, a DMA controller, a serial module, a queued serial peripheral interface, and a timer.

The IMB is the backbone of the MC68341, and is similar to traditional external buses with address, data, clock, interrupt, arbitration, and handshake signals. Because bus masters (like the CPU32 and DMA), peripherals, and the SIM41 are on the same processor, the IMB ensures that communication between these modules is fully synchronized and that arbitration and interrupts can be handled in parallel with data transfers, greatly improving system performance. Internal accesses across the IMB can be monitored from outside of the processor.

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SYSTEM INTEGRATION MODULE

The MC68341 system integration module (SIM41) handles a wide array of functions, eliminating the need for much of the glue logic which typically supports the microprocessor and its interface with peripherals and external memory. The SIM41 includes:

- External Bus Interface—Transfers information between the CPU32 or DMA controller and external memory or peripherals by providing up to 32 address lines and 16 data lines. Both the 68300 bus interface and the original MC68000 bus interface are provided.
- System Configuration and Protection—Achieves maximum system protection by providing various monitors and timers to prevent system lockup, recover from catastrophic failure, exit infinite loops, provide refresh, etc.
- Clock Synthesizer—Generates the clock signals used by all internal operations as well as a clock output used by external devices.
- Chip Select and Wait State Generation—Offers eight programmable chip selects which provide signals to enable external memory and peripheral circuits and create all external handshaking and timing signals. Up to six wait states can be automatically inserted.
- Interrupt Control—Provides up to seven discrete interrupt inputs for external devices.
- IEEE 1149.1 Test Access Port (JTAG)—Aids in system diagnostics by providing dedicated, user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability.
- Real Time Clock—The real time clock can be sustained on a separate power supply for battery backup. This simple counter is driven by 32.768 KHz clock for low power consumption. The real time clock counts seconds, minutes, hours, days, day of the week, date of the month, and year with leap year compensation. The real time clock has internal interrupt generation capability and includes a programmable output pin, which can provide an interrupt or other output signal based upon an alarm or time matching function. Software calibration eliminates the need for an external trim capacitor.

QUEUED SERIAL PERIPHERAL INTERFACE (QSPI) MODULE

The QSPI eases peripheral expansion or interprocessor communications. This function allows interface to and control of other integrated controllers (such as, MC6805 or MC68HC11 family devices) and peripherals (such as, LCD drivers, A/D–D/A converters, digital signal processors, EEPROM). The QSPI can handle up to 16 serial transfers of 8 to 16 bits each or transmit a stream of data up to 256 bits long without CPU intervention, because of a small RAM in the QSPI. A special wrap-around mode allows the QSPI to continuously sample a serial peripheral, automatically updating the QSPI RAM for efficient interfacing to serial analog-to-digital converters.

TIMER MODULE

The timer consists of a 16-bit countdown counter with an 8-bit countdown prescaler for a composite 24-bit resolution. The finest resolution of the timer is 80 ns with a 25-MHz system clock (125 ns @ 16.78 MHz). The programmable timer operating modes are input capture, output compare, square-wave generation, variable duty-cycle square-wave generation, variable-width single-shot pulse generation, event counting, period measurement, and pulse-width measurement.

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POWER CONSUMPTION MANAGEMENT

The MC68341 is very power efficient due to its advanced 0.8-μ HCMOS process technology and its static logic design. The resulting power consumption is typically 500 mW in full operation—far less than the comparable discrete component implementation the MC68341 can replace. For applications employing reduced voltage operation, selection of the MC68341V, which requires only a 3.3-V power supply, reduces current consumption by 40–60% in all modes of operation (as well as reducing noise emissions).

COMPACT DISC-INTERACTIVE

The MC68341 was designed to meet the needs of many markets, including compact disc-interactive (CD-I). CD-I is an standard for a publishing medium that will bring multimedia to a broad general audience—the consumer. CD-I players combine television and stereo systems as output devices, with interactive control using a TV remote-control-like device to provide a multimedia experience selected from software titles contained in compressed form on standard compact discs.

The on-chip real-time clock eliminates the need for a separate chip to keep time-of-day. The 68000 bus interface simplifies the use of existing CD-DA and CD-I peripherals and ASICs that were designed for use with the 68000.

The highly integrated MC68341 is ideal as the central processor for CD-I players. It provides the M68000 microprocessor code compatibility and DMA functions required by the *CD-I Green Book* specification as well as many other useful on-chip functions for a very cost-effective solution. The extra demands of full-motion video CD-I systems make the best use of the MC68341 high performance. The MC68341 is CD-I compliant and has been CD-I qualified. With its low voltage operation, the MC68341V is the only practical choice for portable CD-I.

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MORE INFORMATION

The following table identifies the packages, supply voltages, temperature range, and operating frequencies available for the MC68341.

MC68341 Package/Frequency Availability

	Frequency/Volts			
Package	8 MHz/3.3 V	16 MHz/3.3 V	16 MHz/5 V	25 MHz/5 V
Plastic Quad Flat Pack (FT)	✔	✔	✔	✔
Temperature	0–70 °C	0–70 °C	0–70 °C	0–70 °C

The documents listed in the following table contain detailed information on the MC68341. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Documentation

Document Number	Document Name
BR1114/D	*M68300 Integrated Processor Family*
MC68341UM/AD	*MC68341 User's Manual*
M68000PM/AD	*M68000 Family Programmer's Reference Manual*
AN1063/D	*DRAM Controller for the MC68340*
BR729/D	*The 68K Source*
BR1407/D	*3.3 Volt Logic and Interface Circuits*

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